What is claimed is:

1. A display apparatus comprising:

signal lines and scanning lines arranged laterally and longitudinally on an insulating substrate;

display elements formed near respective points of intersection of said signal lines and said scanning lines;

a signal line driving circuit, which is formed on said insulating substrate, configured to drive the signal lines;

a scanning line driving circuit, which is formed on the insulating substrate, configured to drive the scanning lines; and

a graphic controller IC configured to output digital pixel data in order according to the order of driving the signal lines by said signal line driving circuit,

wherein said graphic controller IC outputs a clock signal in a cycle twice as much as that of the digital pixel data, and

the signal line driving circuit and said scanning line driving circuit drive the signal lines and the scanning lines synchronously with the clock signal, respectively.

2. The apparatus according to claim 1,

wherein the graphic controller IC is mounted on the insulating substrate.

3. The apparatus according to claim 1,

wherein the graphic controller IC has a phase adjusting circuit configured to adjust the phase of the digital pixel data and that of the clock signal.

4. The apparatus according to claim 1,

wherein in addition to the clock signal, a synchronization signal, and the digital pixel data, the graphic controller IC outputs a control signal configured to designate the driving start the signal line driving circuit and the scanning line driving circuit.

5. The apparatus according to claim 1,

wherein the graphic controller IC has a pixel data output circuit configured to output the digital pixel data, and

said pixel data output circuit outputs an intermediate-level voltage between a high-level voltage and a low-level voltage of the digital pixel data for a period during which the valid digital pixel data is not outputted.

6. The apparatus according to claim 1,

wherein each of the display element, the signal line driving circuit, and the scanning line driving circuit is formed by using a polysilicon TFT (Thin Film Transistor), and

the graphic controller IC outputs the clock signal having a frequency at which the polysilicon TFT stably operates.

7. The apparatus according to claim 1,

wherein the signal line driving circuit has a level converting circuit for a single-phase input, which converts the level of each signal outputted from the graphic controller IC, and

said level converting circuit converts the signal outputted from the graphic controller IC into a voltage fluctuating on the threshold voltage of an inverter in the signal line driving circuit by a voltage which changes substantially equally in a vertical direction.

8. The apparatus according to claim 7,

wherein the level converting circuit comprises:

a capacitor element whose one terminal is connected to an input terminal;

an inverter connected to the other terminal of the capacitor element; and

an analog switch connected between input and output terminals of the inverter, and

said analog switch is turned on or off to change an input voltage of the inverter by a voltage fluctuating on the threshold voltage of the inverter substantially equally in a vertical direction.

9. The apparatus according to claim 7,

wherein the signal line driving circuit has a frequency dividing circuit configured to sequentially latch the digital pixel data after completion of the level conversion by the level converting circuit on the basis of the clock signal and outputting the data so as to be distributed in parallel, and

the frequency dividing circuit outputs the odd-numbered digital pixel data and the even-numbered digital pixel data adjacent to the data in a cycle twice as much as that the clock signal.

10. The apparatus according to claim 1,

wherein the signal line driving circuit has:

latch circuits provided for driving the signal lines every N lines (N is an integer larger than or equal to 2), whose number is equal to 1/N of the total number of signal lines; and

D/A converters configured to convert the digital pixel data latched by the latch circuit into an analog voltage, and

the graphic controller IC outputs the digital pixel data in accordance with the order of driving the signal lines by the signal line driving circuit.

11. The apparatus according to claim 1,

wherein in addition to the digital pixel data and the clock signal, the graphic controller IC outputs another clock signal, whose phase is shifted from that of the clock signal by a half cycle.

12. A display apparatus comprising:

signal lines and scanning lines arranged laterally and longitudinally on an insulating substrate;

display elements formed near respective points of intersection of said signal lines and said scanning lines;

a signal line driving circuit, which is formed on the insulating substrate, configured to drive the signal lines;

a scanning line driving circuit, which is formed on the

insulating substrate, configured to drive the scanning lines;

a plurality of data buses arranged from substantially the center of one side of the insulating substrate toward both the ends of said side; and

an order control circuit configured to control the order of digital pixel data transmitted through the data buses so that the signal lines are simultaneously driven every plural lines by said signal line driving circuit.

13. The apparatus according to claim 12, further comprising:

a first latch circuit configured to sequentially latch digital pixel data supplied to the respective signal lines arranged every plural lines;

a second latch circuit configured to simultaneously re-latch all of latch data at a point in time when the latching operation by said first latch circuit is finished once;

D/A converting circuits configured to simultaneously convert respective digital pixel data latched by said second latch circuit into analog pixel voltages; and

selecting circuits configured to select the signal lines to which said analog pixel voltages are supplied.

14. The apparatus according to claim 13,

wherein the second latch circuit latches the digital pixel data so as to divide the data into a plurality of groups, and

the D/A converting circuits simultaneously convert the digital pixel data latched by the second latch circuit into the analog pixel voltages every group.

15. The apparatus according to claim 13,

wherein the second latch circuit has first to Nth (N is an integer larger than or equal to 2) latch units, and

the D/A converting circuits simultaneously convert the digital pixel data latched by the first to Nth latch units of the second latch circuit into analog pixel voltages.

16. The apparatus according to claim 12, further comprising:

an address generating circuit configured to generate an address to designate the kind of the display element to which display update is performed;

a first substrate on which the signal lines, scanning lines, display elements, signal line driving circuit, scanning line driving circuit, a writing control circuit, and data buses are formed; and

a second substrate on which a rearranging circuit and the address generating circuit are formed,

wherein when the digital pixel data is supplied from the rearranging circuit to the data bus, prior to the head data of digital pixel data, the address from the address generating circuit is outputted from a pixel data output terminal.

17. The apparatus according to claim 12, further including:

an address generating circuit configured to generate an address to designate range of the display element to which display update is performed;

a first substrate on which the signal lines, scanning lines, display elements, signal line driving circuit, scanning line driving circuit, a writing control circuit, and data buses are formed; and

a second substrate on which a rearranging circuit and the address generating circuit are formed,

wherein the address generated by said address generating circuit is outputted from a pixel data output terminal.

18. A display apparatus comprising:

a memory cell comprising a plurality of 1-bit memories arranged laterally and longitudinally;

a display layer in which display can be variably controlled according to the values of the plurality of 1-bit memories;

a writing control circuit configured to control the writing operation to the memory cell;

a plurality of data buses arranged from substantially the

center of one side of an insulating substrate toward both the ends of said side; and

an order control circuit configured to control the order of digital pixel data to be transmitted on the data buses so that the 1-bit memories are simultaneously driven every plural memories by the writing control circuit.

19. The apparatus according to claim 18,

wherein the plurality of 1-bit memories adjacent to each other consist of one pixel, and

a plurality of 1-bit memories for red, a plurality of 1-bit memories for green, and a plurality of 1-bit memories for blue are provided in one pixel.

20. The apparatus according to claim 18, further including:

a first latch circuit configured to sequentially latch digital pixel data supplied to the respective 1-bit memories arranged every plural memories;

a second latch circuit configured to simultaneously re-latch all of latch data at a point in time when the latching operation of said first latch circuit is finished once;

a bit line driving circuit configured to amplify a voltage of each digital pixel data latched by said second latch circuit; and

selecting circuits configured to select the bit line to supply an output of said bit line driving circuit.

21. The apparatus according to claim 18, further including:

an address generating circuit configured to generate an address to designate a range in which data in the memory cell is rewritten;

a first substrate on which the memory cell, writing control circuit, and data buses are formed; and

a second substrate on which a rearranging circuit and the address generating circuit are formed,

wherein when the digital pixel data is supplied from the rearranging circuit to the data bus, prior to the head data of

digital pixel data, the address is outputted from the pixel data output terminal.

22. The apparatus according to claim 18, further comprising:

an address generating circuit configured to generate an address to designate a range in which data in the memory cell is rewritten;

a first substrate on which the memory cell, writing control circuit, and data buses are formed; and

a second substrate on which a rearranging circuit and the address generating circuit are formed,

wherein the address generated from the address generating circuit is supplied to the first substrate by using an enable signal line transmitted from the second substrate to the first substrate.

23. The apparatus according to claim 13, further including:

a first level converting circuit configured to convert the level of digital pixel data supplied from the outside to data having a first voltage amplitude;

a frequency dividing circuit configured to divide the frequency of the data level-converted by the first level converting circuit;

a second level converting circuit configured to convert the level of data whose frequency is divided by the frequency dividing circuit into data having a second voltage amplitude smaller than the first voltage amplitude, and supplying the converted data to the data bus; and

a third level converting circuit configured to convert the level of data on the data bus into data having a third voltage amplitude larger than the second voltage amplitude, and supplying the converted data to the first latch circuit.

24. The apparatus according to claim 12, further comprising

a phase duty adjusting circuit configured to independently adjust the phase and duty of a sampling clock of digital pixel

data transmitted on the data buses arranged from substantially the center of one side of the insulating substrate toward one end of said side.

25. A display apparatus comprising:

signal lines and scanning lines arranged laterally and longitudinally on an insulating substrate;

display elements formed near respective points of intersection of said signal lines and said scanning lines;

a signal line driving circuit, which is formed on said insulating substrate, configured to drive the signal lines; and

a scanning line driving circuit, which is formed on the insulating substrate, configured to drive the scanning lines,

wherein the signal line driving circuit latches on the state of separating the digital pixel data of a first color in one horizontal line into the odd pixels and the even pixels, and then after passing a prescribed period, latches on the state of separating the digital pixel data of a second color into the odd pixels and the even pixels, and performs D/A conversion for the latched data of said first color, and supplies the D/A converted data to the corresponding signal line, and then after passing a prescribed period, latches on the state of separating the digital pixel data of a third color into the odd pixels and the even pixels, and performs D/A conversion for the latched data of said second color, and supplies the D/A converted data to the corresponding signal line, and then after passing a prescribed period, performs D/A conversion for the latched data of said third color, and then after passing a prescribed period, supplies the D/A converted data to the corresponding signal line.

26. The apparatus according to claim 25,

wherein the signal lines on the insulating substrate are divided into n blocks (n is an integer larger than or equal to 2), and

the signal lines on said insulating substrate are divided into n blocks (n is an integer larger than or equal to 2);

the apparatus further comprising:

a first block circuit configured to latch on the state of separating the digital pixel data of a first color in one horizontal line into the odd pixels and the even pixels, and then after passing a prescribed period, latches on the state of separating the digital pixel data of a second color into the odd pixels and the even pixels, and performs D/A conversion for the latched data of said first color, and supplies the D/A converted data to the corresponding signal line, and then after passing a prescribed period, latches on the state of separating the digital pixel data of a third color into the odd pixels and the even pixels, and performs D/A conversion for the latched data of said second color, and supplies the D/A converted data to the corresponding signal line, and then after passing a prescribed period, performs D/A conversion for the latched data of said third color, and supplies the D/A converted data to the corresponding signal line, by each block;

a second latch circuit configured to simultaneously latch the latched output of all the odd pixels of said first, second and third colors among the latched output of said first latch circuit, by each block;

a third latch circuit configured to simultaneously latch the latched output of all the even pixels of said first, second and third colors among the latched output of said first latch circuit, by each block;

a D/A converter configured to simultaneously convert the latched output of said second and third latch circuit into analog pixel voltages, by each block; and

a selecting circuit configured to provide the analog pixel voltages converted by said D/A converter to the corresponding signal line.

27. An image control semiconductor device comprising:

a VRAM control unit configured to control the reading/writing operation of an image memory to store digital pixel data;

an output order control circuit configured to change output order of said digital pixel data in accordance with the order

of driving signal lines;

a pixel data output unit configured to divide a plurality of signal lines arranged on an insulating substrate into n blocks (n is an integer larger than or equal to 2) and outputting the digital pixel data rearranged by said output order control circuit in parallel to said respective n blocks in parallel; and

a first start pulse output unit configured to output a first start pulse signal to designate the driving start a signal line driving circuit for each of said n blocks,

wherein said pixel data output unit divides said digital pixel data into a plurality of consecutive output data group, and outputs in sequence each of the consecutive output data group by spacing a prescribed period.

28. The device according to claim 27,

wherein said output order control circuit controls output order so that the digital pixel data of a first color in one horizontal line is latched on the state of being separated into the odd pixels and the even pixels, and then after passing a prescribed period, the digital pixel data of a second color is latched on the state of being separated into the odd pixels and the even pixels, and D/A conversion for the latched data of said first color is performed, and the D/A converted data is supplied to the corresponding signal line, and then after passing a prescribed period, the digital pixel data of a third color is latched on the state of being separated into the odd pixels and the even pixels, and D/A conversion is performed for the latched data of said second color, and the D/A converted data is supplied to the corresponding signal line, and then after passing a prescribed period, D/A conversion for the latched data of said third color is performed, and the D/A converted data is supplied to the corresponding signal line.

29. The device according to claim 27, further comprising:

a double frequency clock output unit configured to output a pixel clock having a frequency twice as high as a display frequency of one pixel; and

a phase adjusting unit configured to adjust phase difference between said digital pixel data and said pixel clock.

30. The device according to claim 29, further comprising:

a diving clock output unit configured to output a clock of dividing a pixel clock; and

a second start pulse output unit configured to output a second start pulse signal having a cycle equal to display period of one horizontal line.

31. The device according to claim 27,

wherein said digital pixel data is composed of k bits (k is an integer of 2 or more), and

the device further comprises an output frequency control unit configured to change output frequency and output amplitude of the digital pixel data outputted from said pixel data output unit, based on the inputted operation mode indicating signal.

32. The device according to claim 30,

wherein said operation mode designating signal includes information regarding the invalid bits of the digital pixel data and the bits other than the designated bits of the digital pixel data are fixed to a predetermined logic.

33. The device according to claim 27,

an output frequency control unit configured to change output frequency and output amplitude of the digital pixel data outputted from said pixel data output unit, based on the inputted operation mode indicating signal.

34. The device according to claim 31,

wherein said operation mode indicating signal includes information configured to designate area configured to update the pixel data in display screen, and

said output order control circuit outputs new digital pixel data only for area designated by said operation mode indicating signal.

35. An image control semiconductor device comprising:

a VRAM control unit configured to control the reading/writing operation of an image memory to store digital pixel data;

a readout address generating unit configured to form a readout address of the image memory;

a pixel data output unit configured to divide a plurality of signal lines arranged on an insulating substrate into n blocks (n is an integer larger than or equal to 2) and outputting digital pixel data read out from said image memory in accordance with the address formed by said readout address generating unit in parallel to said n blocks, respectively; and

a first start pulse output unit configured to output a first start pulse signal to designate the driving start the signal lines to the n blocks, respectively,

wherein the readout address generating unit generates read-out address of said image memory so that the digital pixel data in said block is divided into p consecutive outputted small data groups (p is an integer of 2 or more), and each of these small data groups is outputted by spacing a prescribed period.

36. An image control semiconductor device comprising:

a VRAM control unit configured to control read/write for an image memory configured to store digital pixel data;

a read-out address generator configured to generate read address of said image memory;

first order control means configured to divide a plurality of signal lines arranged on an insulating substrate into n blocks (n is an integer larger than or equal to 2) and to read out the digital pixel data corresponding to address generated by said read-out address generator from said image memory, by each of said n blocks;

second order control means configured to change order of the digital pixel data by each of said n blocks read out by said first order control means into p consecutive outputted small data groups (p is an integer of 2 or more), and to output each of these small data groups by spacing a prescribed period; and

a terminal configured to output a start pulse prior to each of the p small data groups.

37. A method configured to drive a display apparatus comprising: signal lines and scanning lines arranged laterally and longitudinally on an insulating substrate; display elements formed near respective points of intersection of the signal lines and the scanning lines; a signal line driving circuit, which is formed on the insulating substrate, configured to drive the respective signal lines; and a scanning line driving circuit, which is formed on the insulating substrate, configured to drive the respective scanning lines,

wherein the digital pixel data of a first color in one horizontal line is latched on the state of being separated into the odd pixels and the even pixels, and then after passing a prescribed period, the digital pixel data of a second color is latched on the state of being separated into the odd pixels and the even pixels, and D/A conversion for the latched data of said first color is performed, and the D/A converted data is supplied to the corresponding signal line, and then after passing a prescribed period, the digital pixel data of a third color is latched on the state of being separated into the odd pixels and the even pixels, and D/A conversion is performed for the latched data of said second color, and the D/A converted data is supplied to the corresponding signal line, and then after passing a prescribed period, D/A conversion for the latched data of said third color is performed, and the D/A converted data is supplied to the corresponding signal line.